changes in form and details may be made without departing from the spirit and scope of the invention.

What is claimed is:

1. A method of forming and planarizing copper layer, comprising the steps of:

providing a substrate;

forming dual damascene trenches in said substrate;

depositing a barrier metal layer on said substrate and in said dual damascene trenches;

depositing a seed layer on top of said barrier metal layer;

electroplating a copper layer on top of said seed layer by means of forward current electroplating;

forming a reverse tone photoresist mask;

removing that part of said copper layer not covered by said reverse tone photoresist mask by means of reverse current electroplating;

stripping of said photoresist;

planarizing by chemical mechanical polishing (CMP) said now exposed copper layer and barrier metal layer; and

sealing said copper layer with a cap layer.

2. The method of claim 1, wherein said dual damascene trenches are patterned into a silicon oxide layer of a silicon semiconductor wafer.

Subal 3. The method of claim 1, wherein removing said copper layer and said barrier metal layer from areas not covered by photoresist is done through electroplating by reverse current.

4. The method of claim 1, wherein said copper layer can be replaced by metals from the group comprising gold, aluminum, tungsten, titanium, or silver.

5. A method of forming and planarizing copper layer, comprising the steps of:

providing a substrate;

forming damascene trenches;

depositing a barrier metal layer on said substrate in said damascene trenches;

depositing a copper layer on said barrier metal layer, filling said damascene trenches;

forming a reverse tone photoresist mask;

etching said copper layer and barrier metal layer from areas not covered by said reverse tone photoresist mask;

stripping of said photoresist;

planarizing by chemical mechanical polishing (CMP) said now exposed copper layer and barrier metal layer; and

sealing said copper layer with a cap layer.

6. The method of claim 5, wherein said substrate is a silicon oxide layer of a silicon semiconductor wafer.

7. The method of claim 5, wherein said copper layer is removed using a dry anisotropic etch with chlorine (Cl_2) as an etchant.

8. The method of claim 5, wherein said copper layer is removed using a wet isotropic etch with nitric acid (HNO_3) as an etchant.

9. The method of claim 5, wherein said copper layer can be replaced by metal layers from the group comprising gold, aluminum, tungsten, titanium, or silver.

10. The method of claim 5, wherein said reverse tone photoresist mask is a photoresist mask covering that part of said copper layer which is in said trench.

11. The method of claim 5, wherein said reverse tone photoresist mask also covers spaces between said damascene trenches having a separation of less than a critical distance.

12. The method of claim 11, wherein said critical distance ranges from 0.05 μm to 0.2 μm.